HAT880

DUAL POWER BYPASS ATS CONTROLLER

COMMUNICATION PROTOCOL

SMARTGEN (ZHENGZHOU) TECHNOLOGY CO.,LTD.

Chinese trademark

English trademark

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Table 1 - Software Version

Date	Version	Note
2019-05-03	1.0	Original release.

CONTENT

1 OVERVIEW

This protocol describes read and write command format of PC serial port and the definition of internal information data for the third-party to develop and use.

MODBUS communication protocol allows the module to transfer information and data effectively with PLC, RTU, SCADA system of international brands (such as, Schneider, Siemens, and Modicon), and DCS or third-party monitoring system compatible with MODBUS. The monitoring system can be set up if only adding central communication master software (such as Kingview, Intouch、FIX、Synall) basing on PC (or IPC).

2 MODBUS BASIC RULES

- All communication loops should follow the master-slave mode. If so, data can be transferred between a master (e.g. PC) and 32 slaves.
- No communication can start from slaves.
- In communication loop, all communication should be transmitted in “information frame”.
- If received information frame contains unknown command, there is no response.

3 DATA FRAME FORMAT

Communication is asynchronously transferred, using byte (data frame) as unit. Between master and slave, every transmitted data frame is 10-bit (stop bit: 1) or 11-bit (stop bit: 2) serial data stream.

Table 2 - Data Frame Format

Item	Description
Start bit	1-bit
Data bit	8-bit
Parity bit	No parity
Stop bit	1-bit or 2-bit can be set.
Baud rate	2400/4800/9600/19200bps

4 COMMUNICATION PROTOCOL

4.1 INTRODUCTION

When communication command is sent to the slave, corresponding slave receives the communication command, then removes address code, and read the information. If no mistakes, it will execute commands, and sends the result back to the master. Response information includes address code, function code, data and error check code (CRC). If an error occurred in receipt of the command, it will send no information.

4.2 INFORMATION FRAME FORMAT

Table 3 - Information Frame Format

Initiating structure	Address code	Function code	Data field	CRC	End structure
Delay (equivalent to 4 bytes' time)	1 byte 8-bit	1 byte 8-bit	N bytes N*8-bit	2 bytes 16-bit	Delay (equivalent to 4 bytes' time)

4.3 ADDRESS CODE

Address code is the first data frame (8-bit) in each transmitted information frame, 0-255. Single device address range is 1–255, this byte shows that the slave defined by users will recieve the information sent by the master. Each slave has a unique address code, and responses begin with the address code. A master addresses a slave by placing the slave address in the address field of the message. When the slave sends its response, it places its own address in this address field of the response to let the master know which slave is responding.

4.4 FUNCTION CODE

4.4.1 INSTRUCTION

This is the second byte of each transmission. ModBus communication protocol defined function code as 1-255 (01H-0FFH). HAT780 ATS controller uses part of them. Master sends the request and the slave executes actions accoding to the fuction code. If the function code sent by slave is same as that sent by master, it means the response is active. But if the function code MSB is 1 (function code range>127), it means there is no respose or respose has error.

The following table shows the specific signification and operation of function code.

Table 4 - Modbus Partial Function Code

Function code	Definition	Operation
03H	Read Holding Registers	Reads the contents of holding registers.
05H	Force Single Coil	Forces a single coil to either ON or OFF.
06H	Preset Single Register	Write a 16-bit value into a single holding register.

4.4.2 03H READ HOLDING REGISTERS

With fuction code 03H command, the master can read the numerical registers inside the device (numerical registers contains various analog and parameter setting values). Input register values of function code 03H mapping data field are 16 bits (2 bytes). So, from the device reads registers values are 2 bytes. Maximum number of readable registers is 125 each time.

The slave received command format is slave address, function code, data field and the CRC code. The data of data field is in double bytes with every two bytes for a group, and high byte is in advance.

4.4.3 05H FORCE SINGLE COIL

Master uses this command to save a single coil data into bit registers in the device (such as ATS transfer control). The slave also uses this function code to foldback information to the master.

4.4.4 06H PRESET SINGLE REGISTER

Master uses this command to save a single register data into registers in the device. The register data in the ModBus communication is 16-bit (2 bytes) and the first byte contains the high order bits and

the second contains the low order bits. Thus all the points of device are all 2 bytes. Command format is slave address, function code, data field and the CRC code.

4.5 DATA FIELD

4.5.1 INSTRUCTION

Data fields are varies with different function codes.

4.5.2 FUNCTION CODE (03H) –READ HOLDING REGISTERS.

Table 5 - Master Request

Data sequence	Data signification	Byte count
1	Starting address	2
2	Read registers	2

Table 6 - Slave Response

Data sequence	Data signification	Byte count
1	Loopback byte count	1
2	N - register data	N

4.5.3 FUNCTION CODE (05H) –FORCE SINGLE COIL

Table 7 - Master Request

Data sequence	Data signification	Byte count
1	Coil address	2
2	Forced single coil value	2

Table 8 - Slave Response

Data sequence	Data signification	Byte count
1	Coil address	2
2	Single coil value	2

4.5.4 FUNCTION CODE (06H) –PRESET SINGLE REGISTER

Table 9 – Master Request

Data sequence	Data signification	Byte count
1	Register address	2
2	Register value (2-byte)	2

Table 10 – Slave Response

Data sequence	Data signification	Byte count
1	Register address	2
2	Register value (2-byte)	2

4.6 ERROR CHECK CODE (CRC)

The Error Check Code allows the receiving device to detect a packet that has been corrupted with transmission errors. Sometimes, the transmission information occurs imperceptible changes due to

electronic noise and other interference and the CRC code ensure the error information does not work to increase the system's safety and efficiency.

When the CRC is appended to the message, the low-order byte is appended first, followed by the high-order byte.

Note: All information frame format are same: address code, function code, data area and CRC code.

The CRC field is two bytes, containing a 16-bit binary value. The CRC value is calculated by the transmitting device, which appends the CRC to the message. The receiving device recalculates a CRC during receipt of the message, and compares the calculated value to the actual value that received in the CRC field. If the two values are not equal, an error results.

The CRC is started by first preloading a 16–bit register to all 1's. Then a process begins of applying successive 8–bit bytes of the message to the current contents of the register. Only the eight bits of data in each character are used for generating the CRC. Start and stop bits do not apply to the CRC.

During generation of the CRC, each 8–bit character is exclusive ORed with the register contents. Then the result is shifted in the direction of the least significant bit (LSB), with a zero filled into the most significant bit (MSB) position. The LSB is extracted and examined. If the LSB was a 1, the register is then exclusive ORed with a preset, fixed value. If the LSB was a 0, no exclusive OR takes place.

This process is repeated until eight shifts have been performed. After the last (eighth) shift, the next 8–bit byte is exclusive ORed with the register's current value, and the process repeats for eight more shifts as described above. The final contents of the register, after all the bytes of the message have been applied, is the CRC value.

A procedure for generating a CRC-16 is:

- Load a 16–bit register with FFFF hex (all 1's). Call this the CRC register.
- Exclusive OR the first 8–bit byte of the message with the low–order byte of the 16–bit CRC register, putting the result in the CRC register.
- Shift the CRC register one bit to the right (toward the LSB), zero–filling the MSB. Extract and examine the LSB.
- (If the LSB was 0): Repeat Step 3 (another shift).
- (If the LSB was 1): Exclusive OR the CRC register with the polynomial value A001 hex (1010 0000 0000 0001).
- Repeat Steps 3 and 4 until 8 shifts have been performed. When this is done, a complete 8–bit byte will have been processed.
- Repeat Steps 2 through 5 for the next 8–bit byte of the message. Continue doing this until all bytes have been processed.
- The final contents of the CRC register are the CRC value. Least Significant Byte first. When the 16–bit CRC (two 8–bit bytes) is transmitted in the message, the low-order byte will be transmitted first, followed by the high-order byte.

Note: The calculating of CRC code starts from＜slave address＞ and except for all bytes of <CRC code>.

4.7 EXAMPLES OF INFORMATION FRAME FORMAT

4.7.1 FUNCTION CODE 03H

Slave address is 01 and starting address is 3 registers of 0026H (each data is 2 bytes).

Table 11 - Data Address Example

Address	Data(Hex)
0026H	0014
0027H	0014
0028H	0005

Table 12 – Function Code 03H Master Request Example

Request	Bytes	Example (Hex)
Slave address	1	01 Send to the slave 01
Function code	1	03 Read Holding Registers
Starting address	2	00 Starting address is 0026H 26
No. of Points	2	00 Read 3 registers (total 6 bytes) 03
CRC code	2	E4 CRC code which calculated by PC. 00

Table 13 – Function Code 03H Slave Response Example

Response	Bytes	Example (Hex)
Slave address	1	01 Respond to the slave 01
Function code	1	03 Read register
Read count	1	06 3 registers (total 6 bytes)
Data 1	2	00 The content of address 0026H 14
Data 2	2	00 The content of address 0027H 14
Data 3	2	00 The content of address 0028H 05
CRC code	2	91 CRC code which calculated by slave. 71

4.7.2 FUNCTION CODE 05H

Read coil for slave address is 01 and starting address is 0002H. 0002H is addressed as 1.

Table 14 - Coil Data Address Example

Address	Data(Hex)
0000	0
0001	1
0002	0

Note: A value of FF 00 hex requests the coil to be ON. A value of 00 00H requests it to be OFF. All other values are illegal and will not affect the coil.

Table 15 - Function Code 05H Master Request Example

Request	Bytes	For example (Hex)
Slave address	1	01 Send to the slave 01
Function code	1	05 Force single coil
Starting address	2	00 Starting address for 0000H 00
Data	2	FF Set coil as 1 00
CRC code	2	CD CRC code which calculated by PC. FB

Table 16 - Function Code 05H Slave Response Example

Slave response	Bytes	For example (Hex)
Slave address	1	01 Respond to the slave 01
Function code	1	05 Force single coil
Starting address	2	00 Starting address is 0000H 00
Data	2	FF Set coil as 1 00
CRC code	2	CD CRC code which calculated by slave. FB

4.7.3 FUNCTION CODE 06H

Slave address is 01 and starting address is one register of 00E3H(content is 0002H).

Table 17 - Function Code 06H Master Request Example

Request	Bytes	Example (Hex)
Slave address	1	01 Send to the slave 01
Function code	1	06 Preset Single Register
Starting address	2	00 Starting address is 00E3H E3
Data	2	00 Preset Register Data (2 bytes) 02
CRC code	2	F9 CRC code which calculated by PC. FD

Table 18 - Function Code 06H Master Request Example

Slave response	Bytes	For example (Hex)
Slave address	1	01 Respond to the slave 01
Function code	1	06 Preset Single Register
Starting address	2	00 Starting address is 0026H E3
Data	2	00 Preset Register Data (2 bytes) 02
CRC code	2	F9 CRC code which calculated by PC. FD

4.8 ERROR HANDLING

When device detected other errors except the CRC code, the slave must send information to the master. The function code MSB is 1, which means the response function code by slave should add 128 based on the function code.The following codes show that unexpected errors have occurred.

CRC error received from the master will be ignored by the device.

Table 19 - Error Code Format Responded By Slave(CRC excluded)

Type	Byte
Address code	1 byte
Function code	1 byte (MSB is 1)
Error code	1 byte
CRC code	2 bytes

Error code:

01 illegal function code

The function code received in the query is not an allowable action for the slave.

02 illegal data address

The data address received in the query is not an allowable address for the slave.

03 illegal data value

A value contained in the query data field is not an allowable value for the slave.

5 ADDRESS AND DATA

5.1 FUNCTION CODE 03H MAP DATA FIELD

Table 20 - Function Code 03H Map Data Field

Address(decimal)	Item	Description	Bytes Count
0500	Common Alarm	1 for active(LSB)	1bit
	Common Warn Alarm	1 for active	1bit
	Common Fault Alarm	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Audible Alarm	1 for active	1bit
	Reserved	1 for active	1bit
	Auto Mode	1 for active	1bit
	Reserved	1 for active	1bit
	S1 Priority	1 for active	1bit
	S2 Priority	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Genset Start Output	1 for active(MSB)	1bit
0501	S1 Voltage Normal	1 for active(LSB)	1bit
	S1 Voltage Abnormal	1 for active	1bit
	S1 Voltage Instant Abnormal	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	S1 Start Output	1 for active	1bit
	S1 No Volt	1 for active	1bit
	S1 Over Volt	1 for active	1bit
	S1 Under Volt	1 for active	1bit
	S1 Over Freq	1 for active	1bit
	S1 Under Freq	1 for active	1bit
	S1 Loss of Phase	1 for active	1bit
	S1 Phase Sequence Wrong	1 for active	1bit
	Reserved	1 for active(MSB)	1bit
0502	S2 Voltage Normal	1 for active(LSB)	1bit
	S2 Voltage Abnormal	1 for active	1bit
	S2 Voltage Instant Abnormal	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit

Address(decimal)	Item	Description	Bytes Count
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	S2 Start Output	1 for active	1bit
	S2 No Volt	1 for active	1bit
	S2 Over Volt	1 for active	1bit
	S2 Under Volt	1 for active	1bit
	S2 Over Freq	1 for active	1bit
	S2 Under Freq	1 for active	1bit
	S2 Loss of Phase	1 for active	1bit
	S2 Phase Sequence Wrong	1 for active	1bit
	Reserved	1 for active(MSB)	1bit
0503	Breaker Failure	1 for active(LSB)	1bit
	S1 Close Failure	1 for active	1bit
	S1 Open Failure	1 for active	1bit
	Reserved	1 for active	1bit
	S2 Close Failure	1 for active	1bit
	S2 Open Failure	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	S1 Load Over Current Trip	1 for active	1bit
	S2 Load Over Current Trip	1 for active	1bit
	Forced Open Failure Alarm	1 for active	1bit
	S1 Genset Fault	1 for active	1bit
	S2 Genset Fault	1 for active	1bit
	Trip Alarm	1 for active	1bit
	Fail to Synchronize Fault	1 for active	1bit
	Reserved	1 for active(MSB)	1bit
0504	S1 Load Over Current Warn	1 for active(LSB)	1bit
	S2 Load Over Current Warn	1 for active	1bit
	Forced Open Warn	1 for active	1bit
	Battery Under Volt Warn	1 for active	1bit
	Battery Over Volt Warn	1 for active	1bit
	Fail to Synchronize Warn	1 for active	1bit
	Reserved	1 for active	1bit
	Parallel Power Supply	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active(MSB)	1bit

Address(decimal)	Item	Description	Bytes Count
0505	Digital Input 1 Status	1 for active(LSB)	1bit
	Digital Input 2 Status	1 for active	1bit
	Digital Input 3 Status	1 for active	1bit
	Digital Input 4 Status	1 for active	1bit
	Digital Input 5 Status	1 for active	1bit
	Digital Input 6 Status	1 for active	1bit
	Digital Input 7 Status	1 for active	1bit
	Digital Input 8 Status	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active(MSB)	1bit
0506	Relay Output 1 Status	1 for active(LSB)	1bit
	Relay Output 2 Status	1 for active	1bit
	Relay Output 3 Status	1 for active	1bit
	Relay Output 4 Status	1 for active	1bit
	Relay Output 5 Status	1 for active	1bit
	Relay Output 6 Status	1 for active	1bit
	Relay Output 7 Status	1 for active	1bit
	Relay Output 8 Status	1 for active	1bit
	Relay Output 9 Status	1 for active	1bit
	Relay Output 10 Status	1 for active	1bit
	Relay Output 11 Status	1 for active	1bit
	Relay Output 12 Status	1 for active	1bit
	L Supply Output Status	1 for active	1bit
	N Supply Output Status	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active(MSB)	1bit
0507	MS1 Close Control Output	1 for active(LSB)	1bit
	MS1 Open Control Output	1 for active	1bit
	MS2 Close Control Output	1 for active	1bit
	MS2 Open Control Output	1 for active	1bit
	MS1 Breaker Close Status	1 for active	1bit
	MS2 Breaker Close Status	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Manual Test S1	1 for active	1bit
	Manual Test S2	1 for active	1bit
	Reserved	1 for active	1bit

Address(decimal)	Item	Description	Bytes Count
	Reserved	1 for active	1bit
	Remote Start Load	1 for active	1bit
	Remote Start Off Load	1 for active	1bit
	Mains Start Abnormal	1 for active	1bit
	Scheduled Run	1 for active(MSB)	1bit
0508	Cycle Start	1 for active(LSB)	1bit
	Balance Start	1 for active	1bit
	Priority Start	1 for active	1bit
	Reserved	1 for active	1bit
	Scheduled Not Run	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Start Inhibited	1 for active	1bit
	Reserved	1 for active	1bit
	S1 Close Inhibited	1 for active	1bit
	S2 Close Inhibited	1 for active	1bit
	Wait for S1 to Prepare Close PF Input	1 for active	1bit
	Wait for S2 to Prepare Close PF Input	1 for active(MSB)	1bit
0509	NEL 1 Trip Control	1 for active(LSB)	1bit
	NEL 2 Trip Control	1 for active	1bit
	NEL 3 Trip Control	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Elevator Control	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	AutoTrans./Restore	1 for active	1bit
	Remote Control Inhibited	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active	1bit
	Reserved	1 for active(MSB)	1bit
0510	Reserved	1 for active (LSB)	1bit
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		

Address(decimal)	Item	Description	Bytes Count
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
0511	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
	Reserved		
0512	BPS1 Close Output		
	BPS1 Open Output		
	BPS2 Close Output		
	BPS2 Open Output		
	BPS1 Close Status		
	BPS2 Close Status		
	Bypass Unlocked Output		
	ATSE In Work		
	ATSE In Test		
	ATSE In Isolation		
	ATSE Unlocked Output		
	Bypass In Work		
	Bypass In Test		
	Bypass In Isolation		
	Main Unlocked Input		
	Bypass Unlocked Input		
1000	UAB1	Unsigned	2Bytes

Address(decimal)	Item	Description	Bytes Count
1001	UBC1	Unsigned	2Bytes
1002	UCA1	Unsigned	2Bytes
1003	UA1	Unsigned	2Bytes
1004	UB1	Unsigned	2Bytes
1005	UC1	Unsigned	2Bytes
1006	UA1 Phase	Signed(*10)	2Bytes
1007	UB1 Phase	Signed(*10)	2Bytes
1008	UC1 Phase	Signed(*10)	2Bytes
1009	Freq 1	Signed(*100)	2Bytes
1010	Reserved		2Bytes
1011	Reserved		2Bytes
1012	Reserved		2Bytes
1013	Reserved		2Bytes
1014	Reserved		2Bytes
1015	Reserved		2Bytes
1016	Reserved		2Bytes
1017	Reserved		2Bytes
1018	Reserved		2Bytes
1019	Reserved		2Bytes
1020	UAB2	Unsigned	2Bytes
1021	UBC2	Unsigned	2Bytes
1022	UCA2	Unsigned	2Bytes
1023	UA2	Unsigned	2Bytes
1024	UB2	Unsigned	2Bytes
1025	UC2	Unsigned	2Bytes
1026	UA2 Phase	Signed(*10)	2Bytes
1027	UB2 Phase	Signed(*10)	2Bytes
1028	UC2 Phase	Signed(*10)	2Bytes
1029	Freq2	Signed(*100)	2Bytes
1030	Reserved	Signed	2Bytes
1031	Reserved	Signed(*100)	2Bytes
1032	Reserved	Signed(*10)	2Bytes
1033	Reserved		2Bytes
1034	Reserved		2Bytes
1035	Reserved		2Bytes
1036	Reserved		2Bytes
1037	Reserved		2Bytes
1038	Reserved		2Bytes
1039	Reserved		2Bytes
1040	A Phase Current	Unsigned(*10)	2Bytes
1041	B Phase Current	Unsigned(*10)	2Bytes
1042	C Phase Current	Unsigned(*10)	2Bytes
1043	Reserved	Unsigned(*10)	2Bytes

Address(decimal)	Item	Description	Bytes Count
1044	A Current Phase	Signed(*10)	2Bytes
1045	B Current Phase	Signed(*10)	2Bytes
1046	C Current Phase	Signed(*10)	2Bytes
1047	N Current Phase	Signed(*10)	2Bytes
1048 1049	A Phase Active Power	Signed(*10)	4Bytes
1050 1051	B Phase Active Power	Signed(*10)	4Bytes
1052 1053	C Phase Active Power	Signed(*10)	4Bytes
1054 1055	Total Active Power	Signed(*10)	4Bytes
1056 1057	A Phase Reactive Power	Signed(*10)	4Bytes
1058 1059	B Phase Reactive Power	Signed(*10)	4Bytes
1060 1061	C Phase Reactive Power	Signed(*10)	4Bytes
1062 1063	Total Reactive Power	Signed(*10)	4Bytes
1064 1065	A Phase Apparent Power	Signed(*10)	4Bytes
1066 1067	B Phase Apparent Power	Signed(*10)	4Bytes
1068 1069	C Phase Apparent Power	Signed(*10)	4Bytes
1070 1071	Total Apparent Power	Signed(*10)	4Bytes
1072	A Phase Power Factor	Signed(*100)	2Bytes
1073	B Phase Power Factor	Signed(*100)	2Bytes
1074	C Phase Power Factor	Signed(*100)	2Bytes
1075	Average Power Factor	Signed(*100)	2Bytes
1076	Reserved		2Bytes
1077	Reserved		2Bytes
1078	Reserved		2Bytes
1079	Reserved		2Bytes
1080	Battery Volt	Signed(*10)	2Bytes
1081	Reserved		2Bytes
1082	Reserved		2Bytes
1083	Reserved		2Bytes
1084	Switch Transfer Pre-alarm Delay		2Bytes
1085	Reserved		2Bytes
1086	Reserved		2Bytes
1087	Reserved		2Bytes

Address(decimal)	Item	Description	Bytes Count
1088	S1 Voltage Status	See Voltage Status Description	2Bytes
1089	S1 Voltage Status Delay		2Bytes
1090	S2 Voltage Status	See Voltage Status Description	2Bytes
1091	S2 Voltage Status Delay		2Bytes
1092	Genset Status	See Genset Status Description	2Bytes
1093	Genset Status Delay		2Bytes
1094	ATS Status	See ATS Status Description	2Bytes
1095	ATS Status Delay		2Bytes
1096	Reserved		2Bytes
1097	Reserved		2Bytes
1098	Reserved		2Bytes
1099	Reserved		2Bytes
1100	Controller Current Time (Year)	Unsigned	2Bytes
1101	Controller Current Time (Month)	Unsigned	2Bytes
1102	Controller Current Time (Day)	Unsigned	2Bytes
1103	Controller Current Time (Week)	Unsigned	2Bytes
1104	Controller Current Time (Hour)	Unsigned	2Bytes
1105	Controller Current Time (Minute)	Unsigned	2Bytes
1106	Controller Current Time (Second)	Unsigned	2Bytes
1107	Reserved		2Bytes
1108	Reserved		2Bytes
1109	Reserved		2Bytes
1110	Reserved		2Bytes
1111	Continue Power Supply Hours	Unsigned	2Bytes
1112	Continue Power Supply Minutes	Unsigned	2Bytes
1113	Continue Power Supply Seconds	Unsigned	2Bytes
1114	Last Continue Power Supply Hours	Unsigned	2Bytes
1115	Last Continue Power Supply Minutes	Unsigned	2Bytes
1116	Last Continue Power Supply Seconds	Unsigned	2Bytes
1117	S1 Total Power Supply Hours(LSB)	Unsigned	4Bytes
1118	S1 Total Power Supply Hours(MSB)		
1119	S1 Total Power Supply Minutes	Unsigned	2Bytes
1120	S1 Total Power Supply Seconds	Unsigned	2Bytes
1121	S2 Total Power Supply Hours(LSB)	Unsigned	2Bytes
1122	S2 Total Power Supply Hours(MSB)		2Bytes
1123	S2 Total Power Supply Minutes	Unsigned	2Bytes
1124	S2 Total Power Supply Seconds	Unsigned	2Bytes
1125	S1 Total Active Power kwh (LSB)	Unsigned	2Bytes
1126	S1 Total Active Power kwh (MSB)	Unsigned	2Bytes
1127	S1 Total Reactive Power kVarh (LSB)	Unsigned	2Bytes
1128	S1 Total Reactive Power kVarh (MSB)		2Bytes
1129	S1 Total Close Times(LSB)	Unsigned	2Bytes
1130	S1 Total Close Times(MSB)	Unsigned	2Bytes

Address(decimal)	Item	Description	Bytes Count
1131	S 2 Total Active Power kwh (LSB)	Unsigned	2Bytes
1132	S2 Total Active Power kwh (MSB)		2Bytes
1133	S2 Total Reactive Power kVarh (LSB)	Unsigned	2Bytes
1134	S2 Total Reactive Power kVarh (MSB)		2Bytes
1135	S2 Total Close Times(LSB)	Unsigned	2Bytes
1136	S2 Total Close Times(MSB)		2Bytes
1137	Reserved	Unsigned	2Bytes
1138	Reserved		
1139	Reserved	Unsigned	4 Bytes
1140	Reserved		
1141	Reserved	Unsigned	2Bytes
1142	Reserved	Unsigned	2Bytes
1143	Reserved	Unsigned	4 Bytes
1144	Reserved		
1145	Reserved	Unsigned	4 Bytes
1146	Reserved		
1147	Reserved	Unsigned	4 Bytes
1148	Reserved		
1149	Reserved	Unsigned	4 Bytes
1150	Reserved		
1151	S1 Bypass Total Close Times(LSB)	Unsigned	4 Bytes
1152	S1 Bypass Total Close Times(MSB)		
1153	S2 Bypass Total Close Times(LSB)	Unsigned	4 Bytes
1154	S2 Bypass Total Close Times(MSB)		
1155	Reserved	Unsigned	2Bytes
1156	Reserved	Unsigned	2Bytes
1157	Reserved	Unsigned	2Bytes
1158	Reserved	Unsigned	2Bytes
1159	Reserved	Unsigned	2Bytes

5.2 FUNCTION CODE 05H MAP DATA FIELD

Table 21 – Fucntion Code 05H Map Data Field

Address	Item	Description
15000	Remote Close MS1	1 for active, 0 for inactive
15001	Remote Open MS1	1 for active, 0 for inactive
15002	Remote Close MS2	1 for active, 0 for inactive
15003	Reserved	
15004	Auto/Manual	0: Manual 1: Auto
15005	S1 Master	0: Slave 1: Master
15006	S2 Master	0: Slave 1: Master
15007	Alarm Reset	1 for active
15008	Remote Start Genset 1	1 for active
15009	Remote Stop Genset 1	1 for active
15010	Remote Start Genset 2	1 for active
15011	Remote Stop Genset 2	1 for active
15012	Remote Output 1 Output	1 for active
15013	Remote Output 2 Output	1 for active
15014	Remote Output 3 Output	1 for active
15015	Remote Output 4 Output	1 for active
15016	Remote Output 5 Output	1 for active
15017	Remote Output 6 Output	1 for active
15018	Remote Output 7 Output	1 for active
15019	Remote Output 8 Output	1 for active
15020	Remote Output 9 Output	1 for active
15021	Remote Output 10 Output	1 for active
15022	Remote Output 11 Output	1 for active
15023	Remote Output 12 Output	1 for active
15024	Reserved	
15025	Reserved	
15026	Reserved	
15027	Reserved	
15028	Reserved	
15029	Reserved	
15030	Remote BPS1 Close	1 for active, 0 for inactive
15031	Remote Bypass Open	1 for active, 0 for inactive
15032	Remote BPS2 Close	1 for active, 0 for inactive
15033	Reserved	1 for active, 0 for inactive
15034	Remote Master/Bypass Selection	1 for active, 0 for inactive
15035	Reserved	
15036	Reserved	

5.3 S1 VOLTAGE STATUS DESCRIPTION

Table 22 - S1 Voltage Status Description

Count	Status	Delay	Note
0	S1 Normal Identify	Delay (Unit:s)	
1	S1 Abnormal Identify	Delay (Unit:s)	
2	S1 Volt Normal	No Delay	
3	S1 No Volt	No Delay	
4	S1 Over Volt	No Delay	
5	S1 Under Volt	No Delay	
6	S1 Over Freq	No Delay	
7	S1 Low Freq	No Delay	
8	S1 Loss of Phase	No Delay	
9	S1 Phase Sequence Wrong	No Delay	

5.4 S2 VOLTAGE STATUS DESCRIPTION

Table 23 – S2 Voltage Status Description

Count	Status	Delay	Note
0	S2 Normal Identify	Delay (Unit:s)	
1	S2 Abnormal Identify	Delay (Unit:s)	
2	S2 Volt Normal	No Delay	
3	S2 No Volt	No Delay	
4	S2 Over Volt	No Delay	
5	S2 Under Volt	No Delay	
6	S2 Over Freq	No Delay	
7	S2 Under Freq	No Delay	
8	S2 Loss of Phase	No Delay	
9	S2 Phase Sequence Wrong	No Delay	

5.5 GENSET STATUS DESCRIPTION

Table 24 – Genset Status Description

Count	Status	Delay	Note
0	Start Delay	Delay (Unit:s)	
1	Stop Delay	Delay (Unit:s)	
2	Scheduled No Run	Delay (Unit:s)	
3	Scheduled Run	Delay (Unit:s)	
4	S1 Cycle Running	Delay (Unit:s)	
5	S2 Cycle Running	Delay (Unit:s)	
6	S1 Genset Start	No Delay	
7	S2 Genset Start	No Delay	
8	Genset Start	No Delay	
9	Genset Standby	No Delay	
10	Reserved	No Delay	
11	Reserved	No Delay	

5.6 BREAKER STATUS DESCRIPTION

Table 25 - Breaker Status Description

Count	Status	Delay	Note
0	Ready to Transfer	No Delay	
1	MS1 Closing	Delay (Unit:s)	
2	MS1 Opening	Delay (Unit:s)	
3	MS2 Closing	Delay (Unit:s)	
4	MS2 Opening	Delay (Unit:s)	
5	Transfer Rest Time	Delay (Unit:s)	
6	MS1 Again Close	Delay (Unit:s)	
7	MS1 Again Open	Delay (Unit:s)	
8	MS2 Again Close	Delay (Unit:s)	
9	MS2 Again Open	Delay (Unit:s)	
10	Wait to Synchronize	Delay (Unit:s)	
11	MS1 Synchronize to Close	Delay (Unit:s)	
12	MS2 Synchronize to Close	Delay (Unit:s)	
13	Wait for MS1 PF Input	Delay (Unit:s)	
14	Wait for MS2 PF Input	Delay (Unit:s)	
15	Elevator Control Delay	Delay (Unit:s)	
16	MS1 Load Supply	No Delay	
17	MS2 Load Supply	No Delay	
18	Load disconnect	No Delay	
19	BPS1 Closing	Delay (Unit:s)	
20	BPS1 Opening	Delay (Unit:s)	
21	BPS2 Closing	Delay (Unit:s)	
22	BPS2 Opening		
23	BPS1 Load Supply		
24	BPS2 Load Supply		
25	Parallel S1 On Load		
26	Parallel S2 On Load		
27	Reserved		
28	Reserved		
29	Reserved		